Wideband Advanced Recorder and Processor (WARP) Validation Report

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1.0 INTRODUCTION

As spacecraft instruments generate data at ever increasing rates, space systems must find ways to handle that data, and transmit it to the ground stations. This challenge is especially evident on earth-imaging spacecraft employing multispectral and hyperspectral detectors. The Landsat 7 instrument data rate is 150 Mbps. The Earth Observing-1 (EO-1) instrument data rate is over 500 Mbps. The next generation Landsat is expected to have even higher instrument data rates.

EO-1 is a pathfinder to the next generation Landsat mission. A key goal of EO-1 is to pioneer and flight-validate technologies that will make that mission feasible. One of those technologies is the Wideband Advanced Recorder and Processor (WARP). The WARP is essentially a very high data rate solid-state recorder. It is computer-based and provides science and housekeeping data acquisition, storage, and transmission functions. This report describes the EO-1 validated WARP on-board data handling system, its performance, and the resulting lessons learned.

Figure 1 shows the WARP mounted in Bay 1 of the EO-1 spacecraft. Figure 2 shows the WARP's circuit boards. Figure 3 shows the WARP during board-level integration and test. The left board is attached through a connector on the rear of the WARP Backplane. The right board is attached using an extender board. The rear Backplane connector allows testing of an exposed board without the added parasitic inductance and capacitance of an extender board. Boards that are not as sensitive to the parasitic effects can be tested on the extender board. This technique allows two boards to be probed simultaneously during integration and test.

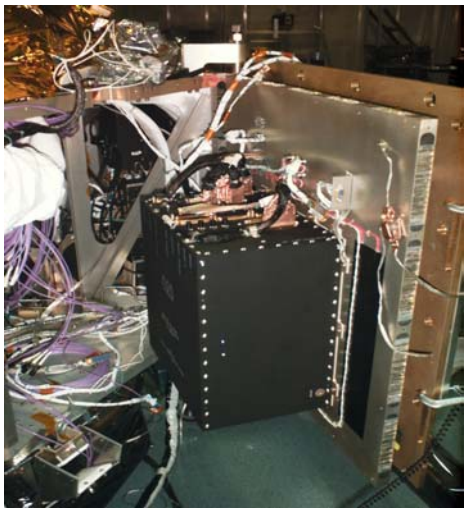

Figure 1. WARP Mounted in Bay 1 of EO-1 Spacecraft

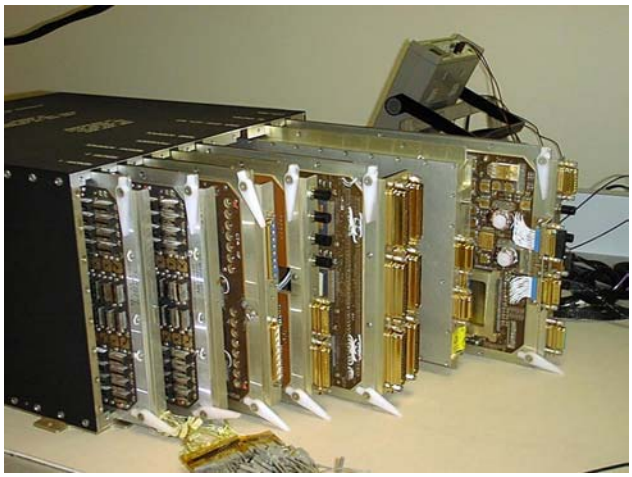

Figure 2. WARP Boards

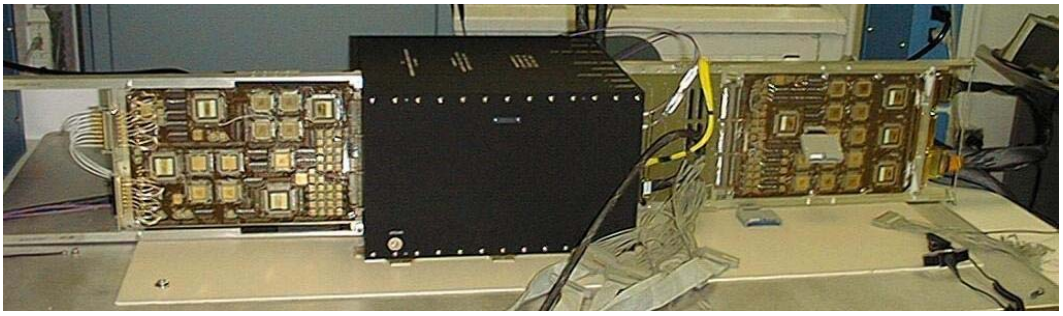

Figure 3. WARP Board-Level Integration and Test

2.0 TECHNOLOGY DESCRIPTION

2.1 EO-1 Flight Data System

Figure 4 shows the science data handling section of the EO-1 Flight Data System. The EO-1 Flight Data System is controlled and monitored through a MIL-STD-1773 Data Bus from an on-board command and data handling (C&DH) unit (not shown). When commanded by the C&DH unit, the instruments acquire ground images (scenes) and transfer those scenes at high rates to the WARP. The WARP stores the scenes as files in bulk memory. When in contact with the ground station, the spacecraft automatically transmits the recorded scenes to the ground station via an X-band downlink or an S-band backup downlink.

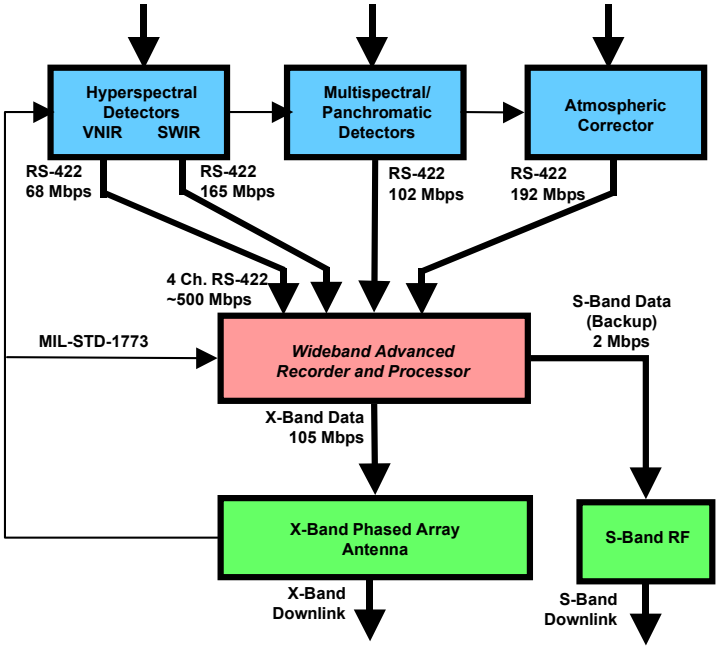

Figure 4. EO-1 Flight Data System Architecture

2.2 Instrument Descriptions

Three revolutionary land imaging instruments on EO-1 collect multispectral and hyperspectral scenes over the course of its mission. The first instrument is the Advanced Land Imager (ALI). The ALI contains

multispectral and panchromatic (MS/PAN) band detectors. The second instrument is the Hyperion. The Hyperion contains two grating imaging spectrometer (GIS) hyperspectral detectors: a Short Wave Infrared (SWIR) band and a Visible and Near Infrared (VNIR) band. The third instrument is the Atmospheric Corrector. The Atmospheric Corrector data is used to compensate for distortions in the acquired science data. The combined continuous data rate from these three instruments is about 500 Mbps. The original baseline mission also featured wedge imaging spectrometer (WIS) hyperspectral detectors that were subsequently deleted. The combined continuous instrument data rate of the original baseline mission was 760 Mbps.

2.3 RF System Description

The primary downlink is through an X-band phased array antenna at 105 Mbps. The downlink has QPSK modulation with separate files being transmitted on the I and Q channels. The transmission is balanced at 52.5 Mbps per channel. EO-1 has a backup downlink through an S-band omni antenna at 2 Mbps.

2.4 WARP Description

Table 1 shows the WARP key specifications. Figure 5 shows the WARP hardware architecture.

Table 1. WARP Key Specifications

Data Storage:	48 Gbits (Easily Expandable to Tera-Bit Range)
Record Rate:	>1 Gbps Burst, 900 Mbps Continuous
Playback Rate:	105 Mbps with built-in X-Band RF Exciter
Data Processing:	Post-Record Capability
Size:	25 x 39 x 37 cm
Mass:	18 kg
Power:	45 W orbit average, 110 W Peak
Thermal:	0-40 °C minimum operating range
Mission Life:	1 year minimum
Radiation:	15 krad total dose, LET 35 MeV

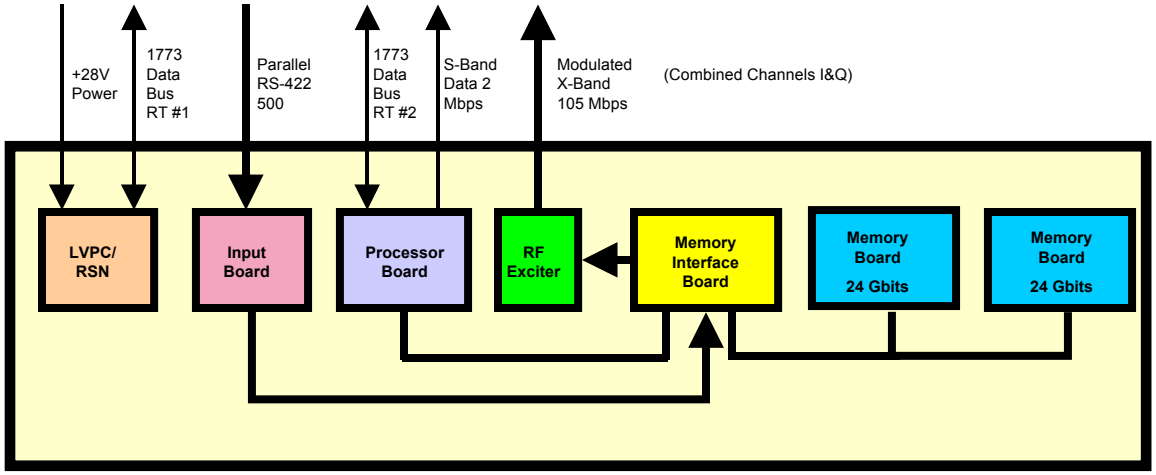

Figure 5. WARP Hardware Architecture

2.4.1 LVPC/RSN Board

The Low Voltage Power Converter / Remote Services Node (LVPC/RSN) is a dual function board. The LVPC converts the + 28 V Primary Spacecraft Power into the required secondary voltages. The RSN is a

microcontroller-based function. It receives commands across the MIL-STD-1773 Data Bus to power on and off certain boards within the WARP, depending on the operational mode. This reduces the WARP's orbital average power. There are four operational modes: Low Power, Data Record, Data Hold and Processing, and X-Band Data Playback. The RSN also acquires housekeeping telemetry within the WARP such as thermistor data, voltage levels, and current levels. The telemetry is transferred back across the MIL-STD-1773 Data Bus to the C&DH Unit.

2.4.2 Data Record Mode

Prior to the initiation of the Data Record Mode, the WARP Processor Board sends commands to the Input Board that select which channels will be recorded. The Processor Board also sends commands to the Memory Interface Board that define where the scene data will be stored in the Memory. Upon receiving the appropriate MIL-STD-1773 command, all the instruments transmit pixel data in bursts across their respective parallel RS-422 interfaces. Each Parallel RS-422 interface consists of 32 data lines and 1 clock line. The Input Board receives the data, filters out appropriate channels and "dead zone" data, rate buffers each channel, and multiplexes each channel into one data stream. It then transmits the data across the 1-Gbps Input Bus to the Memory Interface Board.

The Memory Interface Board receives the input data and breaks the data stream up into fixed length code blocks. It then appends a short Reed-Solomon Error Detection and Correction (EDAC) field to the end of each code block, interleaves the data, and transmits the data stream across the 1-Gbps Memory Data Bus to the Memory Boards. The Reed-Solomon encoding allows radiation induced single event upset bit errors to be corrected on playback. The data interleaving, which spreads code blocks across memory chips, allows data corrections even if entire memory chips fail.

The Memory Boards receive the data stream, generate detailed address locations, and store the data. Each scene of each instrument detector channel is stored in a separate file. Each Memory Board has 24 Gbits of data, organized as six 4-Gbit Arrays. The WARP Memory Board is dual sided. It is implemented with 8-high stacks of 16 Mbit DRAM PEMs. Six Field Programmable Gate Arrays (FPGAs) are used. Due to the very wide data busses that are necessary to handle the 1 Gbps data rate, a significant amount of non-DRAM logic devices are required. To meet the memory density requirements within the fixed printed wiring board real estate, the non-DRAM logic is implemented with wire bond chip-on-board technology. Figure 6 shows a picture of the Memory Board.

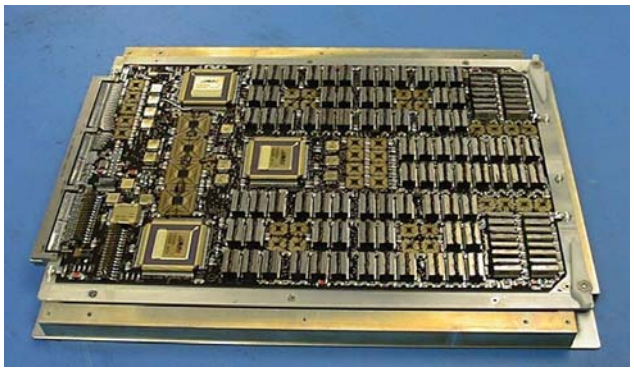

Figure 6. WARP Memory Board

In addition to science data recording, the WARP also records full-resolution instrument housekeeping data across the MIL-STD-1773 Data Bus. The housekeeping data is stored in a memory buffer on the Processor Board until after the science data record is complete. The Processor Board then transmits the

housekeeping data across the 250-Mbps Processor Bus to the Memory Interface Board, which then performs the same operations as it did with the science data stream.

2.4.3 Data Hold and Processing Mode

To maintain the data in memory, the Memory Boards perform DRAM refresh until the data is transmitted to the ground and the file is deleted.

The WARP hardware has the capability of post-processing the science data. However, the post-processing software was never developed due to schedule constraints during the WARP's development. The Processor Board contains a 32-bit, 12-MHz Reduced Instruction Set (RISC) Microprocessor called the Mongoose 5. If developed, the software would use the VxWorks/Tornado Operating System and C programming language. The Processor Board also has a Rice algorithm lossless data compression chip capable of up to a 1.8:1 compression ratio, depending on the image entropy. To post-process the data, the Processor Board would retrieve the desired data from the Memory Boards and re-format the data from the detector focal plane readout order to band-sequential order. Once the data is in band-sequential order, virtually any processing function can be implemented in software. Once the data is processed it would be returned to the Memory Boards. Examples of post-processing functions that were originally intended include thumbnail imaging, cloud detection, radiometric calibration, and data compression.

2.4.4 X-Band Data Playback Mode

The WARP performs X-band data playback by transferring files from the Memory Boards to the Memory Interface Board. The Memory Interface Board de-interleaves the data, performs EDAC on the data using the short Reed-Solomon Decoders, formats the data in accordance with the CCSDS AOS Data Recommendation, appends long Reed-Solomon EDAC coding, and transmits the data to the RF Exciter. Two data streams are transmitted to the RF Exciter, an I channel and a Q channel. The data streams are partitioned such that files are transmitted separately down the I and Q channels.

2.4.5 WARP Technologies

The following technologies were critical to achieve the WARP requirements:

1. Mongoose 5, 32 bit, 12 MHz Microprocessor
2. Essential Services Node Multi-chip Module, 16 bit microprocessor
3. Chip-On-Board Packaging Technology
4. EDAC5HS High Speed (1 Gbps) Reed-Solomon error detection and correction chips, 500 Mbytes per second
5. Universal Source Encoder for Space (USES) chip implementation of the Rice lossless data compression algorithm.
6. Actel 14100 Field Programmable Gate Arrays (FPGAs), 15,000 gates
7. 16 Mbit DRAM, 8 High Stack PEMs
8. VxWorks/Tornado Operating System and C programming language
9. CMOS First In First Out (FIFO) Parts

The above technologies are all available to industry, except for items #2 and #7, which are no longer manufactured. Goddard Space Flight Center (GSFC) developed the first five technologies under the Cross-Enterprise Technology Development Program. GSFC also developed the WARP architecture and designs.

3.0 TECHNOLOGY VALIDATION

3.1 Ground Test Verification

The WARP integration and test (I&T) configuration is show below in Figure 7.

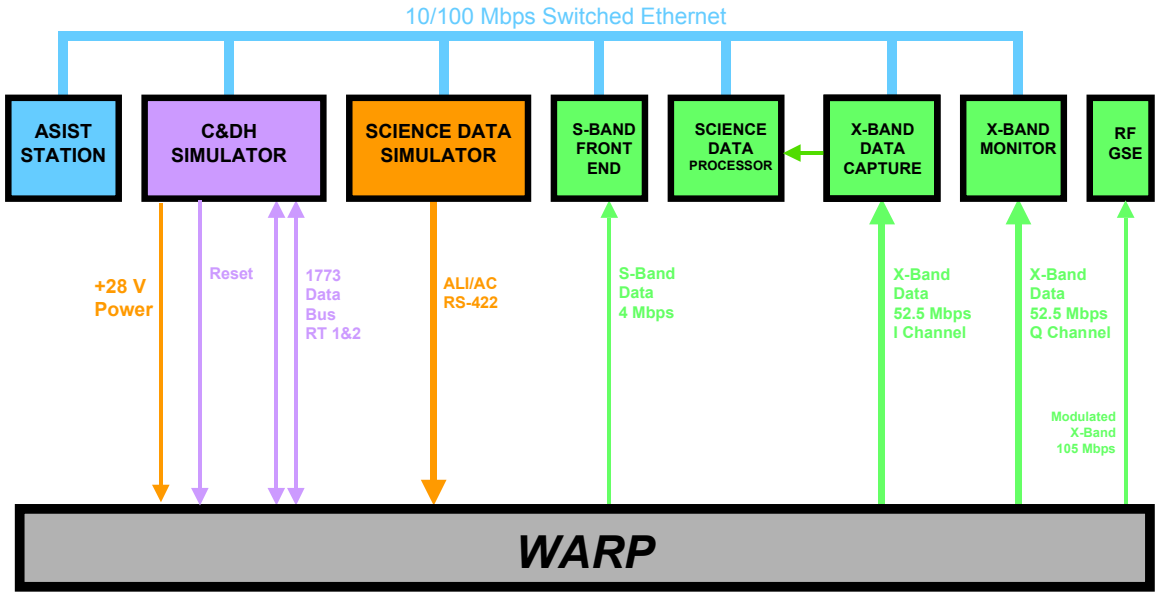

Figure 7. WARP Integration and Test Configuration

The WARP successfully completed a series of ground tests to verify that the WARP performed to its design specification. These tests are described below.

3.1.1 Comprehensive Performance Test (CPT)

This test used several operational scenarios to exhaustively verify all WARP modes, functions, and interfaces. These scenarios typically consisted of WARP power up, data capture, data storage, and downlink. All of the modes and functions of the WARP were exercised.

This test also verified the bit error rate (BER) performance of the WARP. Throughout all of the scenarios of this test, an end-to-end WARP bit error rate was calculated cumulatively on all of the test scenes.

The WARP power and 1773 bus interfaces were exercised in each of the scenarios. The X-Band and S-Band downlink interfaces were each exercised using specific scenarios. X-Band downlinks were performed via both the RF Exciter/GSE and the MIC test port. Several WARP housekeeping functions, such as memory scrubbing, special command processing, and cold/warm restarts, were also exercised in this test.

3.1.2 Limited Performance Test (LPT)

The Limited Performance Test verified the basic WARP functions and interfaces. This test consisted simply of two brief record/playback operations, one using X-Band and the other using S-Band. This test was performed frequently throughout environmental testing to quickly verify that the WARP was still functioning properly.

3.1.3 Normal Operations Test (NOpT)

The Normal Operations Test exercised the WARP over an extended period of time as it was intended to be used on orbit. This test consisted of several sequences of multiple records and X-Band playbacks, thereby simulating operations over a number or orbits. This test was performed during Pre-Environmental Testing and during the Thermal Test.

3.1.4 End-to-End Software Test (ETE)

The End-to-End Software Test was performed as a software regression test. This test included some test cases that were similar to scenarios in the Comprehensive Performance Test. This test, however, went beyond the normal WARP operations to test software functions that are not typically used (i.e. memory dwell, bulk memory reconfiguration, etc.).

3.1.5 Memory Test (MT)

The Memory Test exercised the entire 40 gigabits of WARP memory. This test was performed internally within the WARP where a bit pattern was first written into bulk memory by the Processor Card. The Processor Card then read back the stored value and compared it to the original pattern. Two bit patterns were used to ensure that both a "1" and "0" could be stored in each memory location. MT1 was the memory test using the first pattern and MT2 used the second pattern. Since this was a lengthy test, it was only run during Pre-Environmental Functional and Performance Test, twice during the Thermal cycling Test (one cold plateau and one hot plateau), and once during the Post-Environmental Functional and Performance Test.

3.1.6 Long Duration Storage Test (LDST)

The purpose of the Long Duration Storage Test was to verify the capability of the WARP to store and retain data over an extended period of time and temperature transitions. This test was performed during the Thermal Cycling Test and consisted of loading the entire WARP memory with a data pattern, storing the data for 2 cycles, playing back the data, and verifying that it has not been corrupted.

3.1.7 Cold Start Test (CST)

The Cold Start Test verified the WARP power up at each temperature extreme. This test was performed at the first cold plateau and the first hot plateau (with high input voltage) of the thermal cycling test. In this test, the WARP was powered off after reaching 5^{O}C of the plateau, and soaked until each internal WARP thermistor had reached 0.5^{O}C of the intended plateau and had not changed by more than 0.2^{O}C in one hour. At this point the WARP was powered on and an LPT was performed at both high (35V) and low (21V) primary bus voltage extremes.

3.2 On-Orbit Validation

The WARP was not subjected to any explicit on-orbit tests to validate its performance. Rather, it was put into operational service and monitored for the occurrence of any errors. The WARP performed over 3,000 error-free record and playback operations since the launch of EO-1 in November 2000 to the end of the baseline science mission in November 2001. Its performance has been nominal over that period with the exception of one anomaly that occurred on June 21, 2001.

3.2.1 Anomaly Description

The WARP went into an anomalous state at the end of the day on June 21, 2001 (GMT 2001:172:23:32). The WARP was reporting uncorrectable errors that continued until a reset of the WARP was implemented on the afternoon of June 29, 2001 (GMT 2001:180:20:00). The errors went undetected by the Flight Operations Team because limit checking on the uncorrectable error counter had been unintentionally eliminated. The presence of uncorrectable errors on the WARP caused the science data taken during the anomaly to be mostly unusable.

The anomalous state went undetected until data tapes from the Ground Stations were received at the Mission Operations Center (MOC) and analyzed by Level Zero Data Processing System (DPS) personnel. Tapes from June 21-June 22 began L0 processing on June 27 and the presence of numerous sequence breaks within all files were noted on June 28. Early on June 29, WARP engineers made the following preliminary diagnosis:

- The errors occur only on Memory Card #2 (outermost card).
- The errors occur on all 6 of the 4-Mbit arrays.
- The errors are recurrent.
- There are over 200,000 errors per playback set (about 20% of the data).
- The errors appear to occur in 80 byte blocks.

The engineers prepared an operations instruction to read the WARP Memory Mask register. This test showed that there were no signs of corruption in the register value. Next they ran a WARP Memory Built-In-Test on Memory Card #2 in the range mode. During the course of performing this test, the WARP memory is reformatted. After this, they ran the DCE Self-Test (RS-422 Card Data Injection) that generates card test data. It then became evident that the WARP problem had disappeared and the WARP had returned to a nominal state with no uncorrectable errors. The WARP team filled the entire memory (48 Gbits) and monitored for errors on playback to prove the return to nominal state.

The WARP team attributed the cause of the problem to a radiation induced single event upset, and more specifically to a flipped bit within a state machine inside one of the memory board field programmable gate arrays. An internal review was conducted, and as a result, a limit setting of 1 was instituted for the value of the uncorrectable Error Detection and Correction (EDAC) error counter (i.e., if the value = 1, then the limit is violated and reported to the console operators). The anomaly has not reoccurred since then.

4.0 FUTURE MISSION INFUSION OPPORTUNITIES

Digital electronics technology is advancing so fast that the EO-1 WARP is already obsolete. For example, the WARP has 16 Mbit DRAM chips. Current missions are using 512 Mbit DRAM chips. Also, the WARP has very large parallel RS-422 data inputs that make cross-strapping not feasible. Current missions are using serial interface technology such as Fibre Channel, IEEE 1355, IEEE 1394. Also, the WARP is a single string component. Most new missions require single fault tolerance. There are already solid state recorders on orbit that exceed the data rate and data storage specifications of the WARP. These solid state recorders are readily available from industry.

Future missions using phased array antenna, which by design do not contain a RF Exciter, should consider utilizing the WARP's architecture as shown in Figure 5. This architecture embeds the RF Exciter into the WARP and it worked very well.

5.0 LESSONS LEARNED

1. New technologies, such as the Fiber Optic Data Bus (IEEE-P1393), must be developed independent from flight programs. New technologies require long-term independent research and development (IR&D) modes of development, and cannot be developed as part of a short-cycle flight project.

2. Solid state recorders that can handle extremely high data rates and volume require significant development time. Their development should begin early when the instrument development begins. Otherwise, it will severely impact the mission development schedule.
3. Do not use wire-bonds on boards.
4. Power-up of memory boards must be staggered.
5. Rear backplane connectors were very valuable.
6. Use CRC code in the downlink data format for real-time data quality checking.
7. Provide external box connector for I&T primary power input.

6.0 CONTACT INFORMATION

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7.0 CONCLUSIONS

Figure 8 shows current flight data system technology trends. Instrument data rates are increasing faster than the data system technologies used for handling that data. Bulk data storage technology is advancing rapidly, however the future trend may be inhibited by the radiation tolerance of these ever-shrinking commercial devices. Data Acquisition Interface technology is advancing with several high rate implementations on the horizon. On-board science data processing technology is still in its infancy. Even if it advances, very few scientists are willing to give up the raw data for processed data products. The key bottleneck of the end-to-end data system is the downlink data rate.

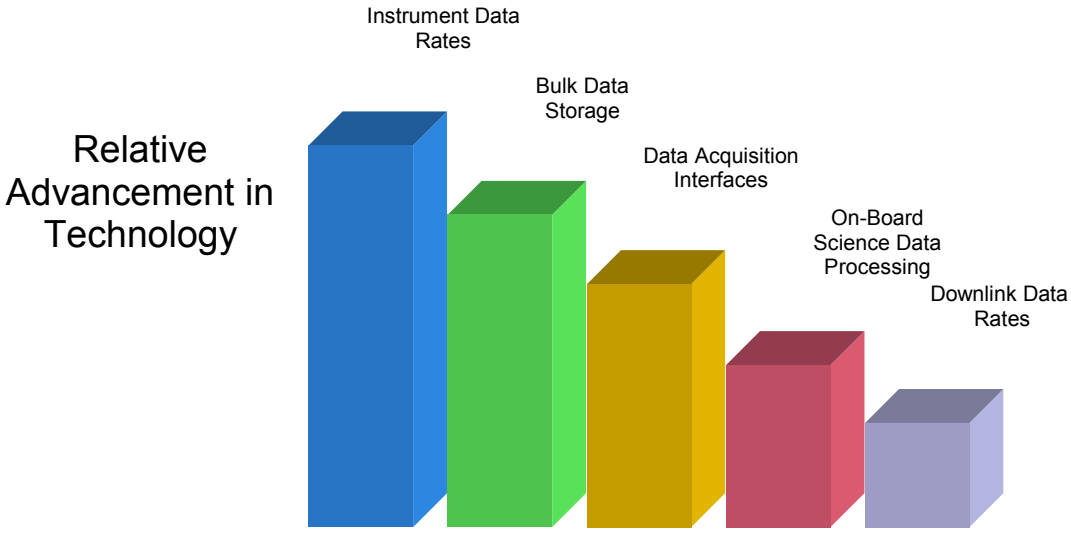

Figure 8. Flight Data System Technology Trends

Given these technologies trends, satisfying the two top-level goals for the next Landsat mission will be difficult. The first goal is for future spacecraft to be much smaller and cheaper than current versions. The second goal is to satisfy the anticipated science community demand for global coverage, full spatial coverage, lossless data compression, wide spectral coverage, and full pixel resolution raw science data. To achieve these two goals, research funds should be put into technologies that increase the downlink data rate and/or contact period.

8.0 ACKNOWLEDGEMENTS

The entire WARP team from Goddard Space Flight Center, Swales Aerospace, Litton Amecon, and Daedalian Systems Corporation is acknowledged for its extraordinary efforts and long hours spent in bringing this technology to fruition.

9.0 REFERENCES

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